REMARKS

The above amendments and these remarks are responsive to the final Office Action issued on February 15, 2006. By this response, claims 1, 9 and 10 are amended. Claims 3, 11-13 and 15-18 are canceled without prejudice. No new matter is added. Claims 1-2, 4-10 and 19 are now active for examination.

The Office Action

The final Office Action dated February 15, 2006 rejected claims 1-13 and 15-18 under 35 U.S.C. §103(a) as being unpatentable over Okado (EP 0511484A2) in view of Hennessy (Computer Architecture) and Holder, Jr. (U.S. Patent No. 5,892,729). Claim 19 was rejected under 35 U.S.C. §103(a) as being unpatentable over Okado in view of Hennessy and Holder, Jr. and further in view of Watanabe (U.S. Patent No. 5,214,786).

It is respectfully submitted that the rejections are overcome in view of the amendments and/or remarks presented herein.

The Rejection of Claims 3, 11-13 and 15-18 is Moot

By this Response, claims 3, 11-13 and 15-18 are canceled without prejudice. Accordingly, the rejection of 3, 11-13 and 15-18 is now moot.

The Obviousness Rejection Based on Okado, Hennessy and Holder, Jr. Is Traversed

Claims 1-2 and 4-10 were rejected as being unpatentable over Okado in view of Hennessy and Holder. By this Response, independent claims 1, 9 and 10 are amended. It is respectfully

submit that the obviousness rejection is overcome because Okado, Hennessy and Holder cannot support a prima facie case of obviousness.

Claim 1, as amended, describes a data processing apparatus comprising an instruction memory in which an instruction is stored, a data memory in which data is stored, and an instruction decoder decoding a fetched instruction. The instruction memory includes a plurality of instruction memory banks. The apparatus further includes a memory operation unit that is coupled to the instruction memory, the data memory and the instruction decoder. The memory operation unit fetches an instruction stored in the instruction memory, and accesses the data memory according to a decode result of the instruction decoder. An integer operation unit is provided to carry out an integer operation according to a decode result of the instruction decoder. The memory operation unit generates (1) a pipeline cycle corresponding to selection of an instruction memory bank to be accessed in a following pipeline cycle, and (2) a pipeline cycle corresponding to an access to an instruction memory bank without any accesses to other instruction memory banks to carry out low power consumption pipeline processing when a plurality of instructions are fetched from the plurality of instruction memory banks. The instruction memory includes a high speed instruction memory, such as cache memory. The memory operation unit generates a pipeline cycle corresponding to instruction readout to carry out a pipeline process when fetching an instruction from the high speed instruction memory. In other words, the number of pipeline stages is rendered variable.

It is respectfully submitted that Okado, Hennessy and Holder, either combined or alone, do not reveal the features of including a high speed memory and generates a pipeline cycle corresponding to instruction readout to carry out a pipeline process when fetching an instruction from the high speed instruction memory, such that the number of pipeline stages is rendered

variable, in combination with other claimed features. Furthermore, there is no objective evidence available in the cited documents providing sufficient motivation to specifically modify the cited documents to provide the structure and functions as described in claim 1. Since Okado, Hennessy and Holder cannot be properly combined, and even if they are combined, the combination does not disclose every limitation of claim 1, the cited documents cannot support a prima facie case of obviousness. The obviousness rejection is untenable and should be withdrawn. Favorable reconsideration of claim 1 is respectfully requested.

Claims 2 and 4-8, directly or indirectly, depend on claim 1, respectively, and incorporate every limitation thereof. Therefore, the obviousness rejection of claims 2 and 4-8, based on Okado, Hennessy and Holder also is untenable and should be withdrawn based on at least the same reasons for claim 1, as well as based on their own merits. Favorable reconsideration of claims 2 and 4-8 is respectfully requested.

By this Response, claim 9 is rewritten into independent form and describes a data processing apparatus comprising an instruction memory, a data memory, an instruction decoder decoding a fetched instruction, and a memory operation unit configured to fetch an instruction stored in the instruction memory, and access the data memory according to a decoded result of the instruction decoder. An integer operation unit is provided to carry out an integer operation according to a decoded result of the instruction decoder. The instruction memory includes a plurality of instruction memory banks. The memory operation unit generates a pipeline cycle corresponding to selection of an instruction memory bank to be accessed in a following pipeline cycle and a pipeline cycle corresponding to an access to an instruction memory bank without any accesses to other instruction memory banks to carry out a low power consumption pipeline processing when a plurality of instructions are fetched from the plurality of instruction memory

banks. The memory operation unit reads out data from the data memory via a data input bus, and writes data into the data memory via a data output bus differing from the data input bus. Therefore, an exemplary data processing apparatus according to claim 10 defines two separate buses: a data input bus and a data output bus different from the data input bus, coupled between the memory operation unit and the data memory.

In contrast, Okado only shows two arrows connecting between a single bus 106 and the data memory 101. However, Okado does not disclose two separate buses coupling between the memory operation unit and the data memory, in combination with other features described in claim 9. It is submitted that other documents of record also fail to disclose the features of claim 9. Accordingly, claim 9 is patentable over the documents of record. Favorable reconsideration of claim 9 is respectfully requested.

Claim 10, as amended, describes features relating to generating a pipeline cycle corresponding to selection of an instruction memory bank to be accessed in a following pipeline cycle, and a pipeline cycle corresponding to an access to an instruction memory bank without any accesses to other instruction memory banks to carry out low power consumption pipeline processing when a plurality of instructions are fetched from the plurality of instruction memory banks. The register file comprises a processor status word. The memory operation unit (1) refers to a first flag indicating a first execution cycle of the loop in the processor status word at the first execution cycle, and retains, in the register of the register file, the instruction in the loop of instructions fetched from the instruction memory when the repeat instruction is executed, and (2) refers to a second flag indicating a second execution cycle to a last execution cycle of the loop in the processor status word at the second execution cycle to the last execution cycle, and executes the loop while fetching the instruction retained in the dedicated register. Thus, an

exemplary apparatus of claim 10 utilizes two flags to control the state of the loop. The flags, for instance, identify which cycle (e.g., a first cycle or a second cycle, etc.) is being executed, to determine where an instruction should to be read out at respective states. It is respectfully submitted that the documents of record, either combined or alone, fail to disclose using two flags to control the state of the loop and detailed operations associated with the use of the flags, in combination with other limitations described in claim 10. Accordingly, claim 10 is patentable over the documents of record. Favorable reconsideration of claim 10 is respectfully requested.

The Obviousness Rejection Based on Okado, Hennessy, Holder and Watanabe Is Overcome

Claim 19 depends on claim 10 and was rejected as being obvious over Okado in view of Hennessy and Holder, Jr. and further in view of Watanabe. The obviousness rejection is respectfully overcome because the cited documents cannot support a prima facie case of obviousness.

As discussed earlier relative to claim 10, Okado, Hennessy and Holder, either combined or alone, fail to disclose every limitation of claim 10, the features of which are incorporated into claim 19 by virtue of its dependency. It is respectfully submitted that the additional document, Watanabe, also fails to describe using two flags to control the state of the loop and detailed operations associated with the use of the flags, in combination with other limitations described in claim 10. Therefore, claim 19 is patentable over the combination of Okado, Hennessy, Holder and Watanabe by virtue of its dependency from claim 10, as well as based on its own merits. Favorable reconsideration of claim 10 is respectfully requested.

Conclusion

For the reasons given above, Applicants believe that this application is conditioned for allowance and Applicants request that the Examiner give the application favorable consideration and permit it to issue as a patent. However, if the Examiner believes that the application can be put in even better condition for allowance, the Examiner is invited to contact Applicants' representatives listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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